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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,623	09/19/2003	Vincent J. Zimmer	42.P16802	4015

7590 07/13/2006

EXAMINER	
MARTINEZ, DAVID E	

ART UNIT	PAPER NUMBER
2181	

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DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,623	ZIMMER ET AL.	
	Examiner	Art Unit	
	David E. Martinez	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 6-12* is/are rejected.

7)☒ Claim(s) *3-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz M. Fleming

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
7/7/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species I – Claims 1-12 in the reply filed on 5/30/06 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, 2 and 6-10 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Application Publication No. US 20002/0016862 A1 to Porterfield.

1. With regards to claim 1, Porterfield teaches a method for allocating address space for a computer platform, comprising:

gathering resource requests for a plurality of peripheral devices hosted by the computer platform [paragraph 21];

determining a resource allocation scheme to support the resource requests of the peripheral devices that consumes a minimum amount of address space [paragraphs 21-22]; and

allocating address space for respective peripheral devices-based on the resource allocation scheme that is determined [paragraph 21].

2. With regards to claim 2, Porterfield teaches the method of claim 1, wherein the peripheral devices comprise PCI (Peripheral Component Interconnect) devices [paragraph 21].

3. With regards to claim 6, Porterfield teaches the method of claim 1, wherein the resource requests pertain to peripheral device input/output (I/O) address requests [paragraphs 3 and 21].

4. With regards to claim 7, Porterfield teaches the method of claim 6, wherein the peripheral device I/O address requests are allocated to a portion of platform address space containing
virtual addresses [paragraph 17].

5. With regards to claim 8, Porterfield teaches the method of claim 1, wherein the resource requests pertain to memory onboard peripheral devices that is requested to be mapped into the computer platform address space [paragraph 21].

6. With regards to claim 9, Porterfield teaches the method of claim 1, further comprising determining resource alignment requirements for the resource allocation [paragraph 21].

7. With regards to claim 10, Porterfield teaches the method of claim 1, further comprising performing legacy aliasing, wherein resources are mapped to the address space in a manner that
accounts for legacy device addressing considerations [fig 2 element 84 includes configuration registers element 112 to map address space in order to support ISA (legacy) devices].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. US 20002/0016862 A1 to Porterfield in view of US Patent Application Publication No. US 2004/0215864 A1 to Arimilli et al. (hereinafter Arimilli).

8. With regards to claim 11, Porterfield is silent as to the method of claim 1, further comprising allocating a reserved portion of address space for hot-plug devices. However,

Arimilli teaches allocating a reserved portion of address space for hot-plug devices for the benefit of supporting the configuration/initialization of hot pluggable devices [paragraph 73].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Porterfield and Arimilli to allocate a reserved portion of address space for hot-plug devices for the benefit of supporting the configuration/initialization of hot pluggable devices [paragraph 73].

9. With regards to claim 12, Porterfield is silent as to the method of claim 11, wherein the allocation of the reserved portion of address space for hot-plug devices enables dynamic reallocation of resources in response to the removal or addition of a hot-plug device to the computer platform. However, Arimilli teaches allocating of the reserved portion of address space for hot-plug devices enables dynamic reallocation of resources in response to the removal or addition of a hot-plug device to the computer platform for the benefit or freeing up system resources for other devices to use [paragraphs 84-87].

It would been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Porterfield and Arimilli to allocate the reserved portion of address space for hot-plug devices enables dynamic reallocation of resources in response to the removal or addition of a hot-plug device to the computer platform for the benefit or freeing up system resources for other devices to use.

Allowable Subject Matter

Claims 3-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record along or in combination fail to teach or fairly suggest aggregating the resource requests for PCI devices at a given level of a PCI hierarchy for the computer platform into respective resource request objects, each resource request object having a size corresponding to the aggregated resource requests of the PCI devices to which it corresponds; defining a bin size comprising an address space aperture corresponding to a resource type of the resource requests; and sorting, via a bin-packing algorithm, the resource request objects into appropriate bins to minimize the number of bins required to support the resource requests for all of the PCI devices hosted by the computer platform.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent Application Publication US 2002/0016877 A1, US Patent Numbers: 6,542,953 and 6,587,868 – all to Porterfield teach the same subjet matter as the Porterfield reference used under the 102 rejected above.

US Patent No. 5,894,563 to Saperstein teaches allocating a portion of PCI address space to a requesting peripheral device(s).

US Patent No. 6,823,418 to Langendorf et al. teaches allocating a portion of PCI address space to a requesting virtual device.

US Patent No. 6,678,770 to Sutoh teaches allocating PCI address space to requesting peripheral device(s).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DEM

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